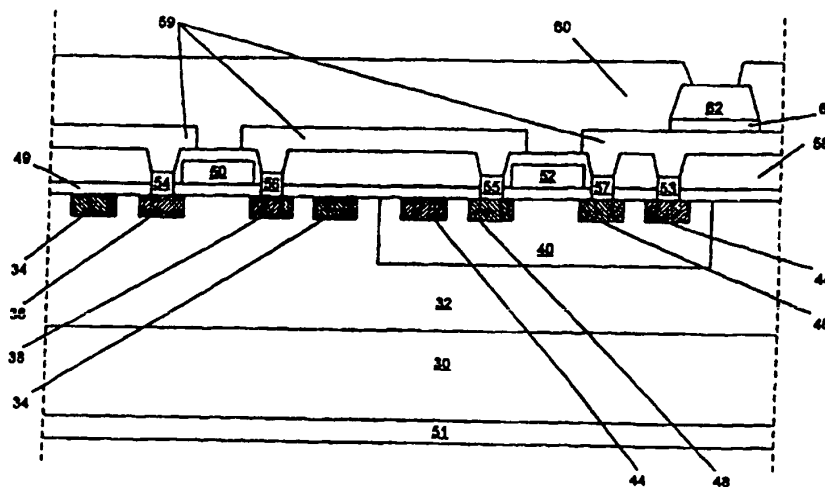




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(54) Title: SILICON CARBIDE CMOS AND METHOD OF FABRICATION



## (57) Abstract

A monolithic CMOS integrated device formed in silicon carbide and method of fabricating same. The CMOS integrated device includes a layer of silicon carbide of a first conductivity type with a well region of a second conductivity type formed in the layer of silicon carbide. A MOS field effect transistor is formed in the well region and a complementary MOS field effect transistor is formed in the silicon carbide layer. The method of fabrication of CMOS silicon carbide includes formation of an opposite conductivity well region in a silicon carbide layer by ion implantation. Source and drain contacts are also formed by selective ion implantation in the silicon carbide layer and the well region. A gate dielectric layer is formed by deposition and re-oxidation. A gate electrode is formed on the gate dielectric such that a channel region is formed between the source and the drain when a bias is applied to the gate electrode. Source drain and body contact are preferably formed of the same material in a single fabrication step.

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## SILICON CARBIDE CMOS AND METHOD OF FABRICATION

This invention was made with Government support and the Government has certain rights in this invention.

### Field of the Invention

5           The present invention relates to metal/polysilicon-oxide semiconductor (MOS) devices formed in silicon carbide. More particularly the present invention related to complementary metal/polysilicon-oxide-semiconductor devices commonly  
10 known as CMOS formed in silicon carbide.

### Background of the Invention

Complimentary MOS (CMOS) integrated devices are monolithically integrated p-channel and n-channel transistors which are optionally interconnected in a  
15 single device. CMOS devices provide the basis for many integrated circuits such as operational amplifiers, sensing devices, digital logic, memory devices, and microprocessors. CMOS technology is readily adaptable to mixed analog and digital applications. The  
20 availability of active or current source loads makes it possible to generate large voltage gains with relatively small supply voltages and currents. CMOS also provides for low power digital circuits. CMOS is also attractive as a technology because lower power  
25 supply voltage operation and reduced circuit design complexity enhances reliability over all operating conditions.

To produce a CMOS device, a single substrate or die must be capable of producing transistors of  
30 complementary type. Thus, a single die must support both p-type and n-type regions to provide for the p-type and n-type channels of the complementary devices.

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Previous CMOS devices have been fabricated in silicon but have not been produced using silicon carbide. The difficulty in fabricating regions of opposite conductivity silicon carbide suitable for producing complementary transistors on a single die or wafer, in addition to the general difficulty in producing a p-channel silicon carbide MOS field effect transistor have prevented production of CMOS in silicon carbide.

Because of the advantages that CMOS integrated devices have over devices comprised solely of p-channel or n-channel transistors, it is desirable to overcome the barriers in silicon carbide to allow for the development of a CMOS silicon carbide integrated device technology.

### Object and Summary of the Invention

In view of the above, it is an object of the present invention to provide a method of fabrication of a monolithic silicon carbide integrated device with a p-channel transistor and an n-channel transistor on the same die or wafer. It is a further object of the present invention to provide a CMOS device formed in silicon carbide.

The methods and structures of the present invention provide an integrated device formed of silicon carbide. The integrated device has a first silicon carbide MOS field effect transistor formed in silicon carbide. This first MOS device has a channel region formed in p-type conductivity silicon carbide. Also in the integrated device is provided a second silicon carbide MOS field effect transistor formed in silicon carbide. This second MOS device has a channel region formed in n-type conductivity silicon carbide. Optionally, the drain of the first silicon carbide MOS field effect transistor is electrically connected to the drain of the second silicon carbide MOS field effect transistor.

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In a preferred embodiment of the present invention the drain and source contacts of the first and second MOS field effect transistors are formed of the same material. The preferred material for these  
5 contacts is nickel.

Preferred structures provided by the present invention include structures for a complementary MOS integrated device which includes a layer of a first conductivity type silicon carbide which may be a  
10 substrate or an epitaxial layer. A well region of a second conductivity type silicon carbide is formed in the silicon carbide layer. A plurality of regions of the second conductivity type silicon carbide are formed in the silicon carbide layer to form a layer source  
15 region and a layer drain region in the silicon carbide layer. A plurality of regions of the first conductivity type silicon carbide are formed in the well region to form a well source region and a well drain region in the well region. A gate dielectric  
20 layer is formed between the layer source and the layer drain regions and extending over at least a portion of the layer drain and layer source regions. Likewise a gate dielectric layer is formed between the well source and the well drain regions and extending over at least  
25 a portion of the well source and well drain regions. A layer gate electrode is formed on the gate dielectric layer formed between the layer source region and the layer drain region so as to provide an active channel region in the first conductivity type silicon carbide  
30 layer between the layer source and the layer drain when a bias is applied to the layer gate electrode. A well gate electrode is also formed on the gate dielectric layer formed between the well source region and the well drain region so as to provide an active channel  
35 region in the second conductivity type well region between the well source and the well drain when a bias is applied to the well gate electrode.

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A well source contact may also be formed on the well source region and a well drain contact may be formed on the well drain region. Similarly a layer source contact may be formed on the layer source region and a layer drain contact formed on the layer drain region.

In an alternate embodiment of the present invention, a plurality of well channel stop regions are formed in the well region. The stop regions are formed of the second conductivity type silicon carbide and have a higher carrier concentration than the well region. The channel stops are positioned such that the well source region and the well drain region are displaced between the channel stop regions. A plurality of layer stop regions may also be formed in the silicon carbide layer adjacent the layer source and the layer drain regions. The layer stop regions are formed of the first conductivity type silicon carbide and have a higher carrier concentration than the silicon carbide layer. The layer stop regions are formed such that the layer source and the layer drain regions are displaced between the layer stop regions.

In addition to the formation of the basic transistor devices, embodiments of the present invention may include an isolation layer formed on the silicon carbide layer, the well region, the well source, gate and drain contacts and the layer source, gate and drain contacts. This isolation layer allows for interconnections of the various silicon carbide devices. This interconnection may be achieved by a plurality of metallization regions for selectively providing connection to the well source, gate and drain contacts and the layer source, gate and drain contacts through connection windows formed in the isolation layer.

In a further embodiment of the present invention, a protective layer is formed on the exposed

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surfaces of the integrated device to protect the device from environmental damage. Connection pads may be formed in a connection pad window through the protective layer to allow for connection to any  
5 underlying region such as the interconnecting metallization.

In a further alternate embodiment of the present invention, at least one of the MOS devices has a source and drain layer region that is self-aligned to  
10 the gate electrode.

The method embodiments of the present invention include a method of forming a complementary MOS integrated device in silicon carbide. The method includes the steps of forming a first silicon carbide  
15 MOS field effect transistor in silicon carbide and having a channel region formed in p-type conductivity silicon carbide and forming a second silicon carbide MOS field effect transistor in silicon carbide which has a channel region formed in n-type conductivity  
20 silicon carbide.

In a particular embodiment of the methods of the present invention, the method of forming a silicon carbide integrated device includes the steps of forming a lightly doped silicon carbide layer of a first  
25 conductivity type having highly doped source and drain regions of a second conductivity type silicon carbide. The second conductivity type is an opposite conductivity type from the first conductivity type. A lightly doped well of the second conductivity type is  
30 formed in the lightly doped layer of the first conductivity type. The lightly doped well has formed in it highly doped source and drain regions of a first conductivity type silicon carbide. Gate dielectric layers are formed on the lightly doped silicon carbide  
35 layer between the source and drain regions of the lightly doped silicon carbide layer of the first conductivity type and on the lightly doped well of the

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second conductivity type between the source and drain regions in the lightly doped well.

In a preferred embodiment of the present invention, the lightly doped well is formed by creating  
5 a masking layer on a surface of the lightly doped silicon carbide layer so as to create a window corresponding to the region of the lightly doped well. Ions are implanted into the lightly doped silicon carbide layer through the window and the implanted well  
10 is annealed to activate the ions implanted in the lightly doped silicon carbide layer to create the lightly doped well of a second conductivity type. Preferably, the ions are implanted at a maximum implant energy of greater than about 250 keV.

15 In a preferred embodiment of the method of forming the drain and source regions, these regions are formed by creating a masking layer on a surface of the lightly doped silicon carbide layer so as to create a window corresponding to the regions of the highly doped  
20 source and drain regions of a second conductivity type. Ions are implanted into the lightly doped silicon carbide layer through the window and the implanted regions are annealed to activate the ions implanted in the lightly doped silicon carbide layer to create the  
25 highly doped source and drain regions of a second conductivity type. Preferably the highly doped source and drain regions of the first conductivity type are formed in the well region and activated in the same manner utilizing an appropriate mask and ion.

30 In a preferred embodiment of the methods of the present invention, the gate dielectric layers are formed by depositing a gate dielectric layer on the surface of the silicon carbide layer with exposed portions of the lightly doped well of a second  
35 conductivity type, the highly doped source and drain regions of a first conductivity type and the highly doped source and drain regions of a second conductivity



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type. The deposited dielectric layer is then heated in an oxidizing ambient.

In a further embodiment of the present invention, gate electrodes are formed on the gate dielectric layers, source contacts are formed on the source regions, and drain contacts are formed on the drain regions. The source contacts and the drain contacts are preferably formed by selective deposition of nickel. The gate electrodes are preferably formed by selective deposition of molybdenum. The formation of the source and drain contacts for both device types is preferably carried out simultaneously.

Stop regions may also be formed surrounding the channel regions and/or source and drain regions by adjusting the mask layer to allow ion implantation in locations surrounding the channel and/or source and drain regions of the device during implantation of the source and drain regions of the complementary device.

In an alternative preferred embodiment an interconnect isolation layer is formed over the gate, source and drain contacts and any exposed gate dielectric layer by deposition of an insulative material. Connections to source, drain and gate electrodes may be made by selectively opening vias in the interconnect isolation layer for contact to the underlying gate, source and drain contacts. A metallization layer may be selectively formed on the interconnect isolation layer to selectively connect the contacts or electrodes of the devices through the opened vias. Successive interconnect isolation layers with corresponding metallization layers and windows to underlying interconnection layers may be formed to provide a multi-layer interconnection system.

Contact pads may also be formed on the metallization to allow contact to probes or wire bonds. A contact pad may be formed by forming a platinum

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region on the metallization layer and forming a gold layer on the platinum region.

A protective layer may also be formed on the device to prevent environmental damage to the device.

5 In such a case windows are opened in the protective layer to allow access to the contact pads.

The foregoing and other objects, advantages and features of the invention, and the manner in which the same are accomplished, will become more readily  
10 apparent upon consideration of the following detailed description of the invention taken in conjunction with the accompanying drawings, which illustrate preferred and exemplary embodiments, and wherein:

#### Description of the Drawings

15 **Figure 1** is a circuit diagram of a CMOS integrated device according to the present invention;

**Figure 2** is a cross-sectional view of a CMOS integrated device according to the present invention;

**Figure 3** is a flow diagram describing the  
20 fabrication sequence for a CMOS device such as that shown in Figure 1;

**Figure 4** is a cross sectional view of an intermediate step in the fabrication of a CMOS integrated device according to the present invention;

25 **Figure 5** is a cross sectional view of an intermediate step in the fabrication of a CMOS integrated device according to the present invention;

**Figure 6** is a cross sectional view of an intermediate step in the fabrication of a CMOS  
30 integrated device according to the present invention;

**Figure 7** is a cross sectional view of an intermediate step in the fabrication of a CMOS integrated device according to the present invention;

35 **Figure 8** is a cross sectional view of an intermediate step in the fabrication of a CMOS integrated device according to the present invention;

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**Figure 9** is a cross sectional view of an intermediate step in the fabrication of a CMOS integrated device according to the present invention;

**Figure 10** is a circuit diagram of a silicon carbide operational amplifier utilizing the present invention;

**Figure 11A** is an I-V Characteristic Plot of an n-channel device according to the present invention;

**Figure 11B** is an I-V Characteristic Plot of a p-channel device according to the present invention;

**Figure 12** is a plot of the DC transfer curve of a CMOS operational amplifier according to the present invention; and

**Figure 13** is a plot of the implant profile of an example of an n-type well according to the present invention.

### Detailed Description

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

**Figure 1** illustrates the basic circuit diagram of a CMOS device according to the present invention. As seen in **Figure 1**, a p-channel MOSFET 20 and an n-channel MOSFET 22 are formed of silicon carbide. These transistors are formed in a single integrated device to create a CMOS integrated device. The transistors shown in **Figure 1** are illustrated with the source/drain region of one device connected to the

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source/drain region of the complementary device. These connections are optional as is the grounding of the source/drain of one transistor and the connection of the second transistor to a voltage source. By

5 connecting the two gate inputs of the transistors it is possible to create a SIC CMOS invertor which is the basic building block of many CMOS digital circuits. The interconnection of the two transistors of **Figure 1** is shown for illustration purposes only.

10 The complementary transistors of **Figure 1** will now be described with reference to **Figure 2** which illustrates one possible cross section for a CMOS silicon carbide integrated device according to the present invention. As shown in **Figure 2**, a bulk single  
15 crystal silicon carbide substrate **30** of a first conductivity type has a lightly doped epitaxial layer **32** of the first conductivity type formed on its upper surface. For purposes of illustration, the first conductivity type may be p-type conductivity silicon  
20 carbide, thus making the epitaxial layer **32** lightly doped p-type ( $p^-$ ) conductivity silicon carbide.

Formed in the epitaxial layer **32** is a well region **40** of a second conductivity type silicon carbide. For purposes of illustration, the second  
25 conductivity type may be n-type conductivity silicon carbide, thus making the well region **40** lightly doped n-type ( $n^-$ ) conductivity silicon carbide.

A plurality of regions of the second conductivity type silicon carbide are formed in the  
30 silicon carbide epitaxial layer **32** to form a layer source region **36** and a layer drain region **38**. These source and drain regions are highly doped regions such that, in the present example, they would be  $n^+$  silicon carbide. A plurality of highly doped second  
35 conductivity type silicon carbide regions **44** are also formed in the well region **40** to create well stop regions. These regions in the present example would

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also be n' silicon carbide. Preferably, the channel stop regions define the perimeter of the device, however, the channel stop regions may only be formed to confine the channel region of the device. Thus, for example, as seen in **Figure 2**, the channel stop regions may be formed only in a third dimension to the cross section show in **Figure 2** such that the channel stop regions run perpendicular to the source and drain regions to confine the channel to the regions between the source and drain regions.

A plurality of regions of the first conductivity type silicon carbide are formed in the well region 40 to form a well source region 46 and a well drain region 48. These source and drain regions are highly doped regions such that, in the present example, they would be p' silicon carbide. The well source region 46 and well drain region 48 are formed within the confines of the well channel stop regions 44. Preferably, the channel stop regions define the perimeter of the device, however, the channel stop regions may only be formed to confine the channel region of the device. Thus, for example, as seen in **Figure 2**, the channel stop regions may be formed only in a third dimension to the cross section show in **Figure 2** such that the channel stop regions run perpendicular to the source and drain regions to confine the channel to the regions between the source and drain regions. A plurality of highly doped first conductivity type silicon carbide regions 34 are also formed in the silicon carbide epitaxial layer 32 to create layer stop regions. These regions in the present example would also be p' silicon carbide. As seen in **Figure 2**, the layer stop regions 34 are formed outside the layer source region 36 and layer drain region 38.

The use herein of the terms "layer" and "well" as prefixes to a feature serves to distinguish

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the features of one transistor from the other, complementary, transistor. For example, a well source region would refer to a region which is associated with the transistor formed in the second conductivity type silicon carbide well. A layer source region refers to a region which is formed in the first conductivity type silicon carbide layer.

Furthermore, while the present invention uses the term "well" to describe the region where the complementary device is formed, as will be appreciated by those of skill in the art, any shaped region of opposite conductivity type silicon carbide may be utilized as long as it is capable of having a complementary silicon carbide device formed in the region. Thus, for example, the "well" region 40 may extend completely through the epitaxial layer 32 to substrate 30 so as to form a contiguous region of second conductivity type silicon carbide which interrupts epitaxial layer 32. Accordingly, the use of the term "well" is used to describe a region where a complementary device may be formed, however that region is created.

Also shown in **Figure 2** is a gate dielectric layer 49 which is formed on the surface of the epitaxial layer 32 opposite the substrate 30. The gate dielectric layer 49 is illustrated as being formed over the entire upper surface of the epitaxial layer 32 with windows opened in the gate dielectric layer 49 over the source and drain regions 36, 38, 46, and 48. However, the gate dielectric layer 49 need only be formed on the epitaxial layer 32 between layer source region 36 and layer drain region 38 and well source region 46 and well drain region 48 with a suitable overlap of the source and drain regions.

As is further illustrated in **Figure 2**, a layer gate electrode 50 is formed on the gate dielectric layer 49 between the layer source region 36

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and layer drain region 38. The layer gate electrode 50 provides an active channel region in the first conductivity type silicon carbide layer between the layer source and the layer drain when a bias is applied to the layer gate electrode. Likewise, a well gate electrode 52 is formed on the gate dielectric layer 49 between well source region 46 and well drain region 48. The well gate electrode 52 provides an active channel region in the second conductivity type well region between the well source and the well drain when a bias is applied to the well gate electrode. While various materials such as poly-silicon may be utilized for forming the gate electrodes, molybdenum is preferred.

Figure 2 further illustrates a layer source ohmic contact 54, a layer drain ohmic contact 56, a well source ohmic contact 57 and a well drain ohmic contact 55 formed on their respective source and drain regions. A well body contact 53 is also shown in Figure 2. These ohmic contacts are preferably formed of the same material and more preferably formed of nickel. However, as will be appreciated by one of skill in the art, ohmic contacts formed on the various conductivity type silicon carbide regions may be formed of different contact materials. Accordingly, nickel may be used to form ohmic contacts to n-type silicon carbide regions and aluminum and/or titanium or platinum may be utilized to form ohmic contacts to p-type silicon carbide regions. Differing contact materials, however, are not preferred because of the increased complexity of fabrication.

Also shown is an ohmic contact 51 formed on the surface of substrate 30 opposite epitaxial layer 32. This layer serves as the layer body contact of the layer device and may be formed of any suitable material for forming an ohmic contact with silicon carbide. In the present example, platinum would be suitable for forming the ohmic contact to the p-type substrate.

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Optionally, the layer body contact may be formed by contacting the epitaxial layer 32 directly.

An interconnect isolation layer 58 is also illustrated in **Figure 2** and may optionally be formed on the exposed surfaces of the integrated device. This isolation layer 58 is formed on the silicon carbide layer 32 to isolate the well region 40, the layer source contact, gate electrode and drain contact 54, 50 and 56 and the well source contact, gate electrode, drain and body contacts 57, 52, 55 and 53. A plurality of metallization regions 59 may also be provided for selective interconnection of the layer source contact, gate electrode and drain contact 54, 50 and 56 and the well source contact, gate electrode and drain and body contacts 57, 52, 55 and 53 through connection windows formed in the isolation layer 58. As shown in **Figure 2**, the drains of the two complementary transistors are connected through a metallization region, however, such is not required by the present invention. Metallization formed of molybdenum is preferred for the present invention, however, other materials such as aluminum may be utilized.

A protective layer 60 may also be formed on the exposed surfaces of the integrated device, such as the metallization regions 59 and the isolation layer 58, to protect the device from environmental damage. Connection pads may also be formed in a connection pad window through the protective layer 60 where the connection pad is selectively formed on the underlying regions such as the metallization regions to provide external contact to the underlying regions. A connection pad is shown in **Figure 2** as a layer of platinum 61 formed on the metallization region 59 in a connection pad window and a layer of gold 62 formed on the layer of platinum 61.

In addition to the general structure above, it is preferred that the gate overlap of the source and



drain regions of the both device types be made as small as possible while still allowing for formation of a channel region between the source and the drain when a bias is applied to the gate electrode. Furthermore, 5 the devices may have self aligned gates for one or both of the devices. Methods of self aligning gates in 3C silicon carbide have been discussed in Palmour et al., J. App. Phys., 64, p. 2168 et seq. (1988) which is incorporated herein by reference as if set forth fully.

10 While the present invention is described above with respect to the formation of the complementary devices in an epitaxial layer formed on a silicon carbide substrate, the present invention is not limited to such a device. For example, the 15 complementary devices may be formed in a silicon carbide substrate with no epitaxial layer. Additionally, there may be additional layers interspersed between a substrate and the silicon carbide layer in which the complementary devices are 20 formed. Accordingly, as used herein the term silicon carbide layer may refer to a layer of silicon carbide formed on a substrate, to a layer of silicon carbide formed on another layer or to a silicon carbide substrate.

25 Also, the above device has been discussed with reference to a p-type epitaxial layer and an n-type well region, a device having an n-type epitaxial layer and a p-type well region may also be utilized. In such a case the first conductivity type silicon 30 carbide would be n-type silicon carbide and the second conductivity type silicon carbide would be p-type silicon carbide. Alternatively, an epitaxial layer of opposite conductivity to a substrate could be used where devices of one channel type are formed in the 35 epitaxial layer and complementary devices formed in the substrate.

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The method of fabrication of devices according to the present invention will now be described with reference to **Figures 3** through 9. Fabrication of CMOS in silicon carbide may be accomplished through a nine step process which includes ion implantation of the source and drain regions of both device-types and the well region for the complementary device. Suitable methods for ion implantation according to the present invention include the high temperature ion implantation methods of commonly assigned United States Patent No. 5,087,576, the disclosure of which is incorporated herein as if set forth fully. These fabrication steps will now be described with reference to fabrication of a silicon carbide device on a p-type epitaxial layer formed on a p-type silicon carbide substrate. However, as described above, the present invention is not limited to devices utilizing a p-type silicon carbide layer but may also be used with n-type silicon carbide layers with suitable substitutions of implantation ions and fabrication techniques based upon the changes in conductivity type. For example, a p-type well region for fabrication of the complementary device could be formed in an n-type silicon carbide layer through implantation of boron ions in the n-type silicon carbide layer.

**Figure 4** illustrates the beginning steps of forming a CMOS integrated device in silicon carbide. After growth of an epitaxial layer on a lightly doped p-type silicon carbide substrate, a mask layer 81 is formed to expose the layer source and drain regions and the well channel stops. The formation of the mask layer is illustrated as block 102 of **Figure 3**. 6H silicon carbide is the preferred polytype for the present invention, however, other silicon carbide polytypes, such as 3C, 4H, and 12H may also be utilized. Preferred carrier concentrations for the p-type

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substrate range from about  $1 \times 10^{16}$  to about  $1 \times 10^{18} \text{ cm}^{-3}$ , however, the doping level of the substrate as it is used in the present example is not critical. Preferred carrier concentrations for the p-type epitaxial layer  
5 range from about  $1 \times 10^{15}$  to about  $1 \times 10^{17} \text{ cm}^{-3}$ . The mask layer may be formed of silicon dioxide ( $\text{SiO}_2$ ), however, any suitable masking material may be utilized.

The masked wafer is implanted with nitrogen ions to form the n' source and drain regions for the n-  
10 channel device and the n' well channel stops for the p-channel device. The implantation step is reflected in block 104 of Figure 3. While nitrogen is the preferred ion for implantation to form the n' regions, other suitable ions known to those of skill may also be  
15 utilized. The nitrogen is preferably implanted at a temperature of  $650^\circ\text{C}$ , however, implantation temperatures ranging from about room temperature to about  $1300^\circ\text{C}$  maybe utilized. The nitrogen is also preferably implanted with multiple implant energies of  
20 not greater than 135 keV with maximum implant energies of less than about 200 keV being suitable. Suitable carrier concentrations for the n' implanted regions are from about  $1 \times 10^{17}$  to about  $1 \times 10^{20} \text{ cm}^{-3}$ .

Figure 5 illustrates that after implantation  
25 of the n' regions the wafer is recoated with polysilicon 82 which is patterned to form an opening in the polysilicon and the underlying oxide mask. The formation of the polysilicon mask is shown in block 106 of Figure 3. This opening corresponds to the n-type  
30 well which provides the opposite conductivity region for the n-channel device. After formation and patterning of the polysilicon/oxide mask, nitrogen is again implanted in the p-type epitaxial layer to form the n' well region 40. Implantation of the well region  
35 is illustrated in block 108 of Figure 3. Nitrogen is the preferred ion for implantation to form the n' well region. The nitrogen is preferably implanted at a

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temperature of 650 °C, however, implantation temperatures ranging from about room temperature to about 1300 °C maybe utilized. The nitrogen is also preferably implanted multiple implant energies with a maximum implant energy of about 380 keV. However, maximum implant energies ranging from about 250 keV to about 1 MeV may be suitable. Suitable carrier concentrations for the n<sup>-</sup> well region is from about  $1 \times 10^{15}$  to about  $1 \times 10^{17} \text{ cm}^{-3}$ . Because of the difficulty of implanting deep wells in silicon carbide and the need to support an application dependent reverse bias voltage, the implant profile of the well region may be tailored such that impurity concentration increases with depth.

After implantation of the n-type well, the wafers are stripped of the mask layers utilizing a wet chemical solution such as hydrofluoric acid or other suitable solutions. The stripping operation is illustrated in block 110 of Figure 3. After stripping, the wafers are annealed to remove damage from caused by ion implantation and to activate the implanted dopants. The wafer is preferably annealed at 1550 °C, however, temperatures ranging from 1000 to about 1800 °C are suitable. The annealing step is shown in block 112 of Figure 3. Optionally, the wafer may be annealed after multiple ion implantations are performed.

After annealing, a third mask layer 83 is formed on the epitaxial layer to create the n-channel stop regions 34 and the p-channel source 46 and drain 48 regions. This mask layer is illustrated in Figure 6. As with the first masking operation, silicon dioxide or any other suitable masking material may be utilized for the mask layer. The formation of the third mask layer is illustrated in Figure 3 at block 114. Aluminum is then implanted to form the p<sup>-</sup> well source and drain regions 46 and 48 and to form the layer stop regions 34. The implantation step is

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reflected in block 116 of **Figure 3**. While aluminum is the preferred ion for implantation to form the p<sup>+</sup> regions, another suitable ion includes boron. The aluminum is preferably implanted at a temperature of about 1200 °C, however, implantation temperatures ranging up to about 1300 °C maybe utilized. The aluminum is also preferably implanted with multiple implant energies of up to about 135 kev with a maximum implant energy being dependent on the depth of the well region. The source and drain region maximum implant energy is limited such that when the source and drain are reverse biased with respect to the well region, the well region beneath the source and drain is not fully depleted and the depletion region below the source and drain does not extend into the substrate. Suitable carrier concentrations for the p<sup>+</sup> implanted regions are from about  $1 \times 10^{17}$  to about  $1 \times 10^{20} \text{ cm}^{-3}$ .

After implantation of the p<sup>+</sup> regions, the third mask is stripped as described above and the wafer is again annealed as described above. This second strip and anneal step is illustrated in block 118 of **Figure 3**. After the second anneal, the wafers may optionally be thermally oxidized to remove surface damage and the resulting oxide again stripped.

After the formation of the n<sup>+</sup> and p<sup>+</sup> regions, the two devices are fabricated in the same manner. As seen in **Figure 7**, the gate dielectric layer 49 is deposited on the epitaxial layer 32 so as to cover the channel regions of the two devices. This gate dielectric layer is preferably silicon dioxide and is deposited and then oxidized as described in commonly assigned United States Patent No. 5,459,107 entitled METHOD OF OBTAINING HIGH QUALITY SILICON DIOXIDE PASSIVATION ON SILICON CARBIDE AND RESULTING PASSIVATED STRUCTURES, and as described in copending and commonly assigned United States Patent Application Serial Number 08/554,319, entitled PROCESS FOR REDUCING DEFECTS IN

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OXIDE LAYERS ON SILICON CARBIDE, filed November 8, 1995, the disclosures of which are incorporated herein by reference as if set forth fully. Thus, after deposition of a silicon dioxide layer, the wafers are  
5 preferably placed in a furnace in an oxidizing ambient for several hours prior to the deposition of gate metal on the gate dielectric 49. This deposit and re-oxidize step is illustrated in block 120 of Figure 3.

While deposition and reoxidation of the gate  
10 dielectric layer is preferred, other methods of forming the gate dielectric layer, such as thermally growth may be utilized. The densified deposited oxide was chosen as the gate insulator to strengthen the gate overlap regions of the device where most MOSFET oxide  
15 reliability failures occur. The deposited oxide eliminates the step that develops at either end of the lightly doped channel during the growth of a thermal gate oxide. This step is the result of an enhanced oxidation rate over the implanted source/drain regions.  
20 The step can act as a field concentrator in the gate overlap regions and stress the gate oxide. The dielectric strength of an oxide which is grown on heavily implanted SiC is poor, and additional stress increases the likelihood of an oxide related failure in  
25 the overlap region. This weakness may be attributed to impurity incorporation, non-stoichiometric growth, or a rough SiC-SiO<sub>2</sub> interface due to impurity segregation or implant damage. A deposited oxide reduces these concerns related to impurity incorporation and  
30 segregation. The incorporation of aluminum in the gate overlap regions of p-channel devices is a particular problem because it creates a deleterious gate leakage path at elevated temperatures. The oxidizing anneal step is performed to ensure proper oxide stoichiometry  
35 and to improve the SiC-SiO<sub>2</sub> interface.

After completion of the formation of the gate dielectric layer 49, the gate metal, 50 and 52, is

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deposited and patterned. This operation is shown in block 122 of **Figure 3**. As discussed above, the gate material is preferably molybdenum, however, other suitable gate materials include polysilicon or  
5 aluminum.

After deposition of the gate material, an isolation layer 58 is deposited on the wafer and vias are etched through the isolation layer to expose portions of the n' and p' source and drain regions or  
10 the well region or the epitaxial layer. The formation of the isolation layer 58 is illustrated in **Figure 8**. The isolation layer 58 is preferably formed of silicon dioxide but may be formed of any suitable insulating material such as silicon nitride. The isolation layer  
15 serves to isolate the devices from an interconnect metallization layer which is formed on the isolation layer. The formation of the isolation layer is reflected in block 124 of **Figure 3**.

After formation and etching of the isolation  
20 layer 58, nickel or other suitable ohmic contact material is deposited in the vias opened in the isolation layer 58 to simultaneously create the source and drain ohmic contacts 54, 56, 55 and 57 and the well region contact 53. While the simultaneous creation of  
25 contacts for both type devices is preferred, the p-type contacts and the n-type contacts could be formed of differing materials and formed in multiple fabrication steps if desired. The contacts are preferably annealed for about 2 minutes at about 825 °C, however, any time  
30 and temperature combination sufficient to form the metal-semiconductor contact may be utilized. The contact formation steps are illustrated in block 126 of **Figure 3**.

After formation of the contacts,  
35 metallization 59 is selectively formed on the isolation layer to selectively connect the devices sources, drains, gates and epitaxial layer or well region. As

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an example, the drains of the two devices illustrated in **Figure 8** are interconnected by metallization formed on the isolation layer. The metallization is preferably formed of molybdenum, however, other  
5 suitable metallization materials such as aluminum may be utilized. The formation and patterning of the interconnection metallization may be done by any suitable technique known to those of skill in the art. The formation of the interconnect metallization is  
10 shown in block 128 of **Figure 3**.

An example of the final device is shown in **Figure 9**. The final steps of fabrication of the device include selectively forming contact pads by depositing a platinum layer 61 and a gold layer 62 on the  
15 metallization layer 59. The formation of the contact pads is shown in block 130 of **Figure 3**. The entire device is then covered with a protective layer 60 to protect the device from the environment. The protective layer 60 is patterned to open vias above the  
20 contact pads to allow for probing or formation of wire bond or other suitable external connections. The protective layer 60 may be a deposited layer of silicon dioxide or other suitable material such as silicon nitride. The formation of the protective layer is  
25 illustrated in block 132 of **Figure 3**.

Described above have been various formation and patterning steps for the creation of masking or isolation or protective layers. These steps may be carried out using any suitable technique for formation  
30 and patterning such as, for example, by chemical vapor deposition or other techniques known to those of skill in the art. Suitable equipment for the formation of the devices utilizing the growth, deposition and implantation techniques described above is commercially  
35 available and known to those of skill in the art.

A CMOS silicon carbide integrated circuit has been fabricated utilizing the present invention. The



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CMOS silicon carbide circuit is illustrated in **Figure 10** and is an operational amplifier. The operational amplifier was formed on a 6H p-type silicon carbide substrate with a p-type epitaxial layer doped to a carrier concentration of from about  $2 \times 10^{15} \text{ cm}^{-3}$  to about  $2 \times 10^{16} \text{ cm}^{-3}$ . The epitaxial layer had a thickness of about 3 to 5  $\mu\text{m}$ . The fabrication techniques described above were carried out to create the complementary devices required for the operational amplifier of **Figure 10**.

The n-well for the p-channel device was created with a 15 V power supply in mind. The high temperature nitrogen implant energy was limited at the time to 380 keV. The worst case condition is having the drain of a p-channel device near ground (the substrate potential) while the n-well is at  $V_{DD}$  which puts 15 V of reverse bias on the well from both directions. To support this bias without punching through the n-wall, the simulated profile shown in **Figure 13** was implemented. A higher implant energy and lower dose may also be utilized to form a deeper and flatter impurity profile which may accomplish the same reverse bias capability. The reverse bias capability may also be reduced to accommodate a  $V_{DD}$  of 12 V, another common supply voltage available in most systems. This would reduce the total dose and energy required to form the n-wells, and would reduce implant damage that occurs in forming the n-well. The dual use of the source/drain implants for channel stops was employed here to simplify this process, however, separate implants with lighter doses and lower energies may also be utilized.

The carrier concentrations of the n' regions of the device were approximately  $1 \times 10^{19} \text{ cm}^{-3}$  and carrier concentrations of the n' well are illustrated in **Figure 13**. The carrier concentration of the p' regions was approximately  $1 \times 10^{18} \text{ cm}^{-3}$ . The n' and p' regions were implanted to a depth of about 0.35 and 0.25  $\mu\text{m}$

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respectively and the source and drain regions had dimensions of about 8  $\mu\text{m}$  by 25  $\mu\text{m}$  to about 100  $\mu\text{m}$ . The n-type wells were formed to a depth of approximately 0.7  $\mu\text{m}$  in the p-type epitaxial layer. Gate widths of approximately 25 to 200  $\mu\text{m}$  and gate lengths of approximately 2 to 8  $\mu\text{m}$  were utilized.

The I-V characteristics of the complementary devices are shown in **Figure 11A** and **Figure 11B**. **Figure 11A** illustrates the operational characteristics of the n-channel device formed in the well region. **Figure 11B** illustrates the operational characteristics of the p-channel devices formed in the epitaxial layer. The threshold voltage of the n-channel devices was 2.5 volts and the threshold voltage of the p-channel devices was about -15 to -17 volts.

**Figure 12** is a graph of the DC transfer curve for the silicon carbide CMOS operational amplifier of **Figure 10**. The open loop operational gain of the amplifier was about  $10^4$  or 80 db.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

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## THAT WHICH IS CLAIMED IS:

1. An integrated device formed in silicon carbide semiconductor material, said integrated device comprising:
  - a first silicon carbide MOS field effect transistor formed in said silicon carbide semiconductor material and having a channel region formed in p-type conductivity silicon carbide; and
  - a second silicon carbide MOS field effect transistor formed in said silicon carbide semiconductor material and integrated with said first transistor wherein said second silicon carbide MOS field effect transistor has a channel region formed in n-type conductivity silicon carbide.
2. A silicon carbide integrated device according to claim 1 wherein the drain of said first silicon carbide MOS field effect transistor is electrically connected to the drain of said second silicon carbide MOS field effect transistor.
3. A silicon carbide integrated device according to claim 1 wherein the drain and source contacts from said first and said second MOS field effect transistors are formed of the same material.
4. A silicon carbide integrated device according to claim 3 wherein said drain and source contacts are formed of nickel.
5. A silicon carbide integrated device according to claim 1 wherein the gate dielectric of said first and said second silicon carbide transistor is a deposited gate oxide.

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6. A silicon carbide integrated device according to claim 1 wherein said first and said second transistors are formed in a silicon carbide epitaxial layer formed on a silicon carbide substrate.

5 7. A complementary MOS integrated device comprising:

a layer of a first conductivity type silicon carbide;

a well region of a second conductivity type  
10 silicon carbide formed in said silicon carbide layer;

a layer source region and a layer drain region of said second conductivity type silicon carbide formed in said silicon carbide layer;

a well source region and a well drain region  
15 of said first conductivity type silicon carbide formed in said well region;

a gate dielectric layer formed between said layer source and said layer drain regions and between said well source and said well drain regions;

20 a layer gate electrode formed on said gate dielectric layer formed between said layer source region and said layer drain region so as to provide an active channel region in said first conductivity type silicon carbide layer between said layer source and  
25 said layer drain when a bias is applied to said layer gate electrode; and

a well gate electrode formed on said gate dielectric layer formed between said well source region and said well drain region so as to provide an active  
30 channel region in said second conductivity type well region between said well source and said well drain when a bias is applied to said well gate electrode.

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8. The silicon carbide integrated device of claim 7, further comprising:

a well source contact formed on said well source region;

5 a well drain contact formed on said well drain region;

a well body contact formed on said well region;

10 a layer source contact formed on said layer source region;

a layer drain contact formed on said layer drain region; and

a layer body contact formed on said layer of silicon carbide.

15 9. The silicon carbide integrated device of claim 7, further comprising:

well channel stop regions formed in said well region wherein said stop regions are formed of said second conductivity type silicon carbide and have a  
20 higher carrier concentration than said well region wherein said well source region and said well drain region are displaced between said channel stop regions; and

layer stop regions formed in said silicon  
25 carbide layer adjacent said layer source and said layer drain regions wherein said layer stop regions are formed of said first conductivity type silicon carbide and have a higher carrier concentration than said silicon carbide layer.

30 10. A silicon carbide integrated device according to claim 7, said integrated device further comprising:

an isolation layer formed on said silicon carbide layer; and

35 metallization regions for selectively providing connection to said well source contact, gate

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electrode, drain and body contacts and said layer source contact, gate electrode, drain and body contacts through connection windows formed in said isolation layer.

5           11. A silicon carbide integrated device according to claim 10, said integrated device further comprising a protective layer formed on the exposed surfaces of said integrated device to protect said device from environmental damage.

10           12. A silicon carbide integrated device according to claim 11, said integrated device further comprising at least one connection pad formed in a connection pad window through said protective layer wherein said connection pad is formed on at least one  
15 of said metallization regions.

13. A silicon carbide integrated device according to claim 12, wherein said connection pad comprises:

          a layer of platinum formed on said  
20 metallization region in said connection pad window; and  
          a layer of gold formed on said layer of  
• platinum.

14. A silicon carbide integrated device according to claim 8, wherein at least one of said  
25 metallization regions connects said well drain contact to said layer drain contact.

15. A silicon carbide integrated device according to claim 10 wherein said metallization is formed of molybdenum.

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16. A silicon carbide integrated device according to claim 8, wherein said layer source and drain contacts and said well source and drain contacts are formed of the same contact material.

5 17. A silicon carbide integrated device according to claim 16 wherein said contact material comprises nickel.

18. A silicon carbide integrated device according to claim 8, wherein at least one of said well  
10 gate electrode, said well source region and said well drain or said layer gate electrode, said layer source region and said layer drain region are self aligned.

19. A silicon carbide integrated device according to claim 7, wherein said well gate dielectric  
15 and said layer gate dielectric layer are formed of silicon dioxide.

20. A method of forming a monolithic complementary MOS integrated device in silicon carbide, the method comprising the following steps:

20 forming a first silicon carbide MOS field effect transistor in silicon carbide wherein the channel region of the first device is formed in p-type conductivity silicon carbide; and

forming a second silicon carbide MOS field  
25 effect transistor in silicon carbide integrated with the first silicon carbide MOS field effect transistor wherein the channel of the second transistor is formed in n-type conductivity silicon carbide.

21. The method of forming a silicon carbide  
30 integrated device according to claim 20, wherein said forming a first silicon carbide MOS field effect transistor and said forming a second silicon carbide

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MOS field effect transistor steps comprise the steps of:

forming a lightly doped silicon carbide layer of a first conductivity type having highly doped source and drain regions of a second conductivity type silicon carbide wherein said second conductivity type is an opposite conductivity type from said first conductivity type;

forming a lightly doped well of said second conductivity in the lightly doped layer having highly doped source and drain regions of a first conductivity type silicon carbide; and

forming gate dielectric layers on the lightly doped silicon carbide layer between the source and drain regions of the lightly doped silicon carbide layer and on the lightly doped well between the source and drain regions of the lightly doped well.

22. The method of claim 21 wherein the first conductivity type silicon carbide comprises p-type conductivity silicon carbide and wherein the second conductivity type silicon carbide comprises n-type conductivity silicon carbide.

23. The method of forming a silicon carbide integrated device according to claim 21, wherein said forming a lightly doped well comprises the following steps:

creating a masking layer on a surface of the lightly doped silicon carbide layer so as to create a window corresponding to the region of the lightly doped well;

implanting ions into the lightly doped silicon carbide layer through the window; and

annealing the implanted well to activate the ions implanted in the lightly doped silicon carbide



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layer to create the lightly doped well of a second conductivity type.

24. The method of claim 22, wherein said implanting step comprises implanting ions at a maximum  
5 implant energy of greater than about 250 keV.

25. The method of forming a silicon carbide integrated device according to claim 21, wherein said forming a highly doped source and drain regions of a second conductivity type comprises the following  
10 steps:

creating a masking layer on a surface of the lightly doped silicon carbide layer so as to create a window corresponding to the regions of the highly doped source and drain regions of a second conductivity type;  
15 implanting ions into the lightly doped silicon carbide layer through the window; and  
annealing the implanted regions to activate the ions implanted in the lightly doped silicon carbide layer to create the highly doped source and drain  
20 regions of a second conductivity type.

26. The method of forming a silicon carbide integrated device according to claim 21, wherein said forming a highly doped source and drain regions of a first conductivity type step comprises the following  
25 steps:

creating a masking layer on a surface of the lightly doped silicon carbide layer so as to create a window corresponding to the regions of the highly doped source and drain regions of a second conductivity type;  
30 implanting ions into the lightly doped silicon carbide layer through the window; and  
annealing the implanted regions to activate the ions implanted in the lightly doped silicon carbide

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layer to create the highly doped source and drain regions of a second conductivity type.

27. The method of forming a silicon carbide integrated device according to claim 21, wherein said forming gate dielectric layers step comprises the steps of:

depositing a gate dielectric layer on the surface of the silicon carbide layer with exposed portions of the lightly doped well of a second conductivity type, the highly doped source and drain regions of a first conductivity type and the highly doped source and drain regions of a second conductivity type; and

heating the dielectric layer in an oxidizing ambient.

28. The method of forming a silicon carbide integrated device according to claim 21 further comprising the steps of:

forming gate electrodes on the gate dielectric layers;  
forming source contacts on the source regions;  
forming body contacts to the layer and the well; and  
forming drain contacts on the drain regions.

29. The method according to claim 28 wherein said source, drain and body contacts are formed of deposited nickel.

30. The method according to claim 28 wherein said gate electrodes are formed of deposited molybdenum.

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31. The method of forming a silicon carbide integrated device according to claim 28 wherein said forming source contacts step and said forming drain contacts step are carried out simultaneously.

5           32. The method of forming a silicon carbide integrated device according to claim 28 wherein said forming gate electrode steps comprises depositing a gate electrode material on the gate dielectric layer between the source and drain regions of the same  
10 conductivity type so as to provide a gate electrode so that a conductivng channel is formed between the drain and the source regions when a bias is applied to the gate electrode.

15           33. The method of forming a silicon carbide integrated device according to claim 28 wherein said forming source contacts and said forming drain contacts steps comprises depositing a contact material on the source and drain regions.

20           34. The method of forming a silicon carbide integrated device according to claim 21 further comprising the steps of:

          forming highly doped regions of a first conductivity type silicon carbide in the lightly doped silicon carbide layer opposite the channel region  
25 formed between the source and drain regions of a second conductivity type to act as channel stop regions for the conductive channel formed between the source and drain regions of a second conductivity type; and

          forming highly doped regions of a second  
30 conductivity type silicon carbide in the lightly doped well of silicon carbide of a second conductivity type opposite the channel region formed between the source and drain regions of a first conductivity type to act as channel stop regions for the conductive channel

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formed between the source and drain regions of a first conductivity type.

35. The method of forming a silicon carbide integrated device according to claim 28 further  
5 comprising the step of forming an interconnect isolation layer on the surface of the device.

36. The method of forming a silicon carbide integrated device according to claim 35 further comprising the steps of:  
10 selectively opening vias in the interconnect isolation layer for contact to the underlying gate electrode, source, drain and body contacts;  
forming a metallization layer on the interconnect isolation layer to selectively connect the  
15 gate electrode, source, drain and body contacts through the opened vias.

37. The method of forming a silicon carbide integrated device according to claim 36 further comprising the step of forming a contact pad on the  
20 metallization.

38. The method of forming a silicon carbide integrated device according to claim 37 wherein said step of forming a contact pad comprises the steps of:  
forming a platinum region on the  
25 metallization layer; and  
forming a gold layer on the platinum region.

39. The method of forming a silicon carbide integrated device according to claim 36 further comprising the step of forming a protective layer on  
30 said metallization layer.

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40. The method of forming a silicon carbide integrated device according to claim 20 wherein said step of forming a lightly doped well of said second conductivity in the lightly doped layer having highly doped source and drain regions of a first conductivity type silicon carbide further comprises the step of implanting boron ions in a layer of silicon carbide of the first conductivity type to form the lightly doped well of said second conductivity type.

10 41. The method of forming a silicon carbide integrated device according to claim 20 wherein said step of forming a lightly doped well of said second conductivity in the lightly doped layer having highly doped source and drain regions of a first conductivity type silicon carbide further comprises the step of  
15 implanting nitrogen ions in a layer of silicon carbide of the first conductivity type to form the lightly doped well of said second conductivity type.

42. A method of forming a silicon carbide  
20 integrated device comprising the steps of:  
forming an epitaxial layer of lightly doped silicon carbide of a first conductivity type on a silicon carbide substrate;  
forming a first mask on the epitaxial layer  
25 having openings corresponding to a source and drain region for a first MOS transistor and channel stop regions for a second MOS transistor;  
implanting ions in the epitaxial layer through the openings in the first mask to create  
30 regions of highly doped silicon carbide of a second conductivity type in the epitaxial layer;  
forming a second mask having an opening corresponding to a well region for formation of the second MOS transistor; then

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implanting ions in the epitaxial layer through the opening in the second mask to create a well region of lightly doped silicon carbide of a second conductivity type;

5 forming a third mask wherein the third mask has openings corresponding to a source and drain region for the first MOS transistor and channel stop regions for the second MOS transistor;

10 implanting ions in the epitaxial layer through the openings in the third mask to create regions of highly doped silicon carbide of a first conductivity type in the epitaxial layer;

annealing the implanted regions to activate the implanted ions;

15 forming a gate dielectric layer on the epitaxial layer;

forming gate electrodes on the gate dielectric between the source and drain regions of the first and second transistors;

20 forming source and drain contacts corresponding to the implanted regions of the source and drain of the first and second transistors; and forming body contacts to the silicon carbide epitaxial layer and the well region.

25 43. The method of Claim 42, further comprising the steps of:

forming an interconnect isolation layer having openings for selectively contacting the source, drain and body contacts and gates of the first and  
30 second transistors;

forming metallization on the interconnect isolation layer and selectively connecting the source, drain and body contacts and gate electrodes of the first and second transistor;

35 forming a protective layer on the integrated device to prevent environmental damage; and

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forming contact pads through the protective layer to provide an external contact to the metallization.

44. The method of forming a silicon carbide integrated device of claim 42 wherein said step of
- 5 implanting ions in the epitaxial layer through the openings in the first mask to create regions of highly doped silicon carbide of a second conductivity type in the epitaxial layer comprises the steps of:
- 10 implanting ions at an implantation energy of up to about 200 keV at a temperature of less than about 1300 °C to provide regions of the second conductivity type silicon carbide having a carrier concentration of greater than about  $1 \times 10^{17} \text{ cm}^{-3}$ ; and then
- 15 annealing the implanted regions at a temperature of from about 1000 to about 1800 °C.

45. The method of forming a silicon carbide integrated device of claim 42 wherein said step of
- 20 implanting ions in the epitaxial layer through the openings in the third mask to create regions of highly doped silicon carbide of a first conductivity type in the epitaxial layer comprises the steps of:
- implanting ions at an implantation energy of up to about 200 keV at a temperature of less than about
- 25 1300 °C to provide regions of the first conductivity type silicon carbide having a carrier concentration of greater than about  $1 \times 10^{17} \text{ cm}^{-3}$ ; and then
- annealing the implanted regions at a temperature of from about 1000 to about 1800 °C.

30

46. The method of forming a silicon carbide integrated device of claim 42 wherein said step of forming a gate dielectric layer on the epitaxial layer comprises the steps of:

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depositing a gate dielectric layer on the surface of the silicon carbide layer with exposed portions of the lightly doped well of a second conductivity type, the highly doped source and drain regions of a first conductivity type and the highly doped source and drain regions of a second conductivity type; and

heating the dielectric layer in an oxidizing ambient.

10           47. The method of forming a silicon carbide integrated device of claim 42 wherein said step of forming source and drain contacts corresponding to the implanted regions of the source and drain of the first and second transistors comprises the steps of:

15           forming the source and drain contacts on the first conductivity type implanted regions of a first contact material; and

            forming the source and drain contacts on the second conductivity type implanted regions of a second  
20 contact material.



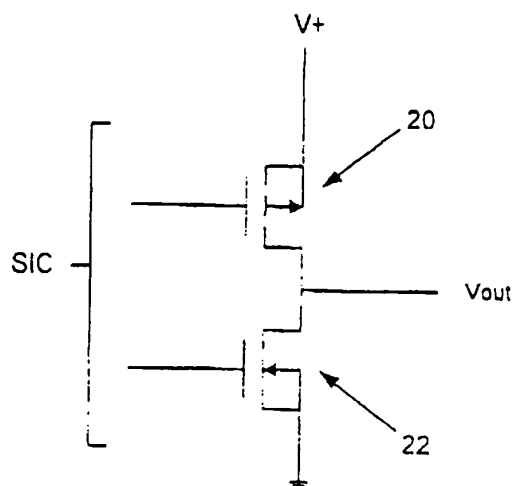


FIGURE 1

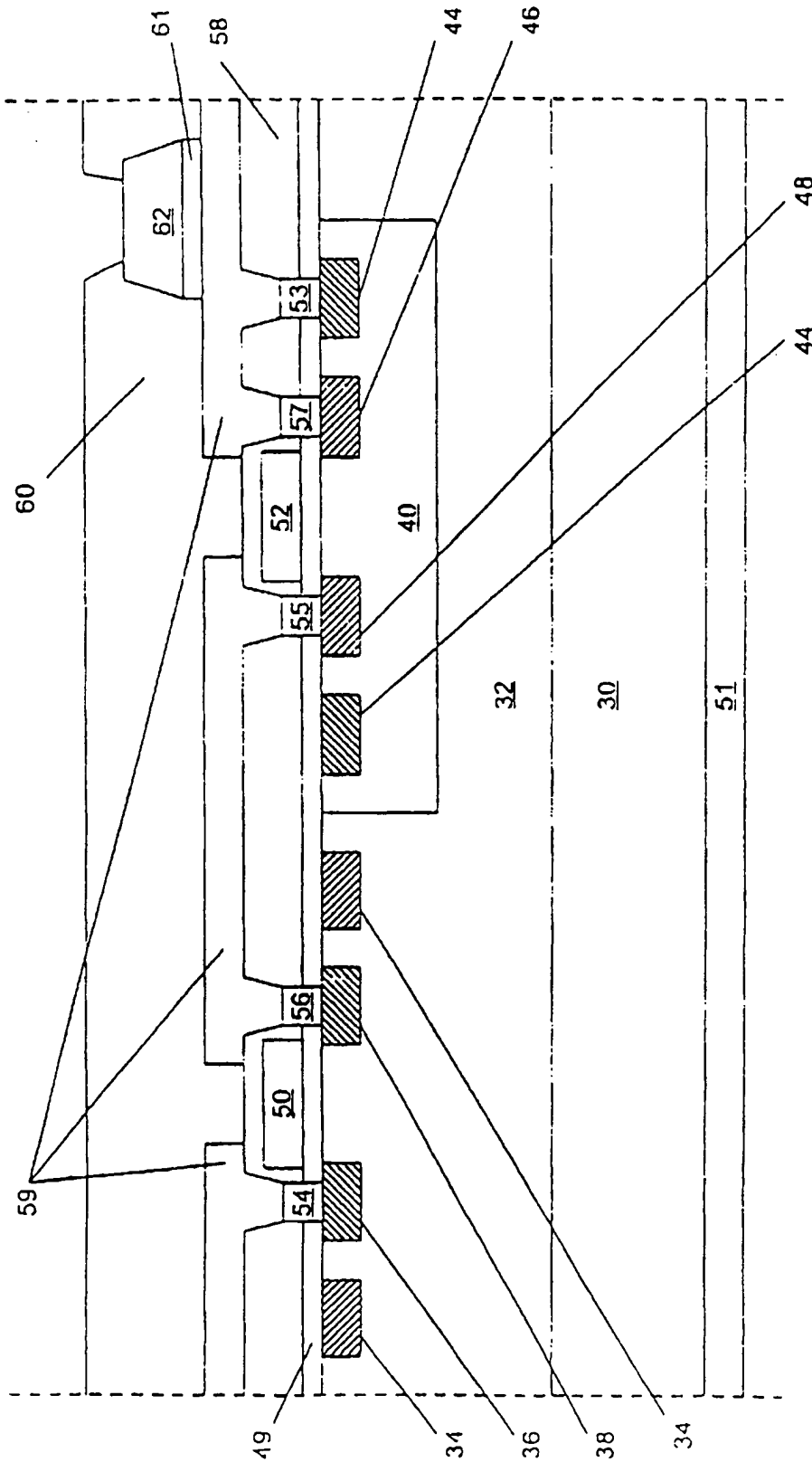


Figure 2

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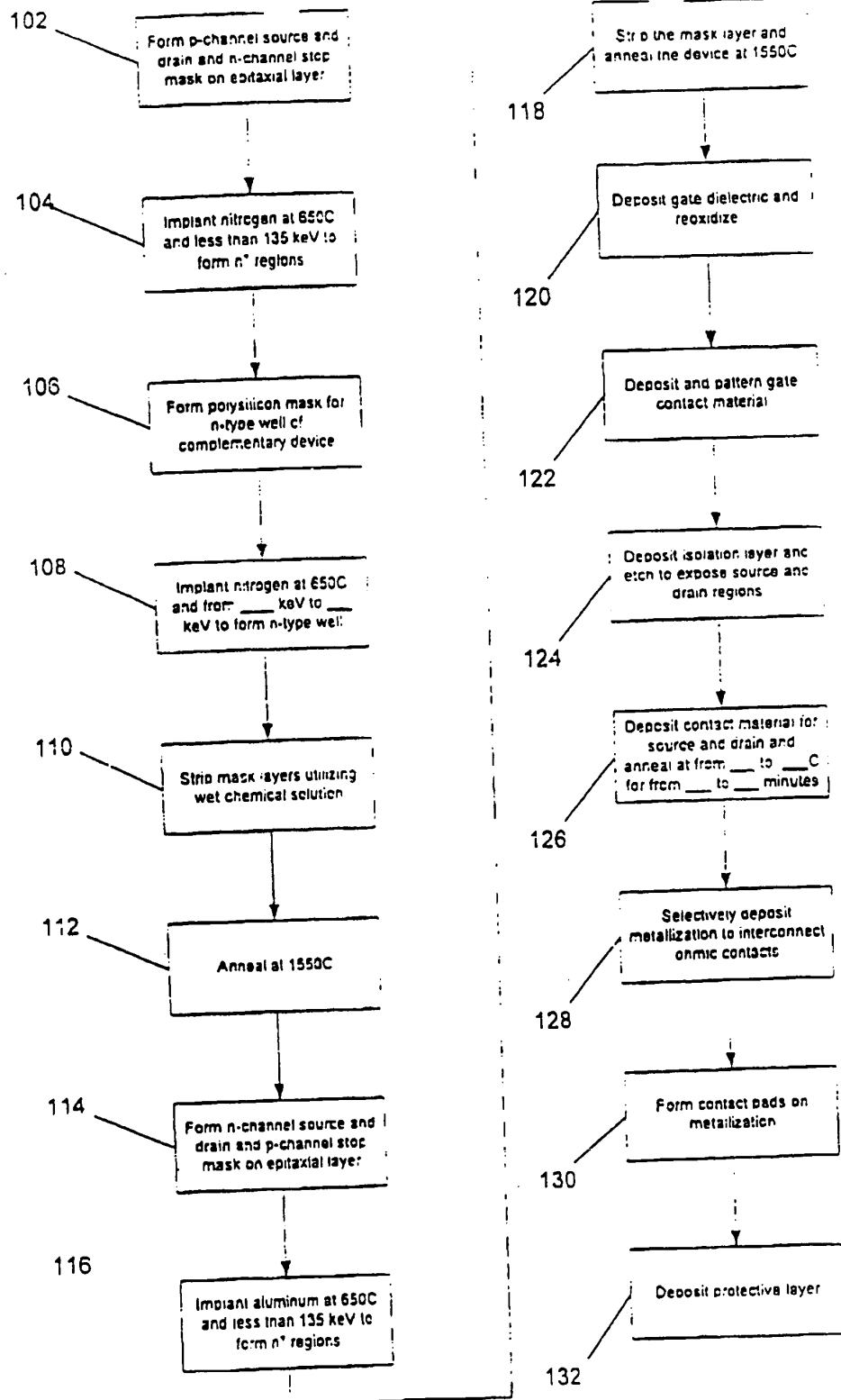


Figure 3

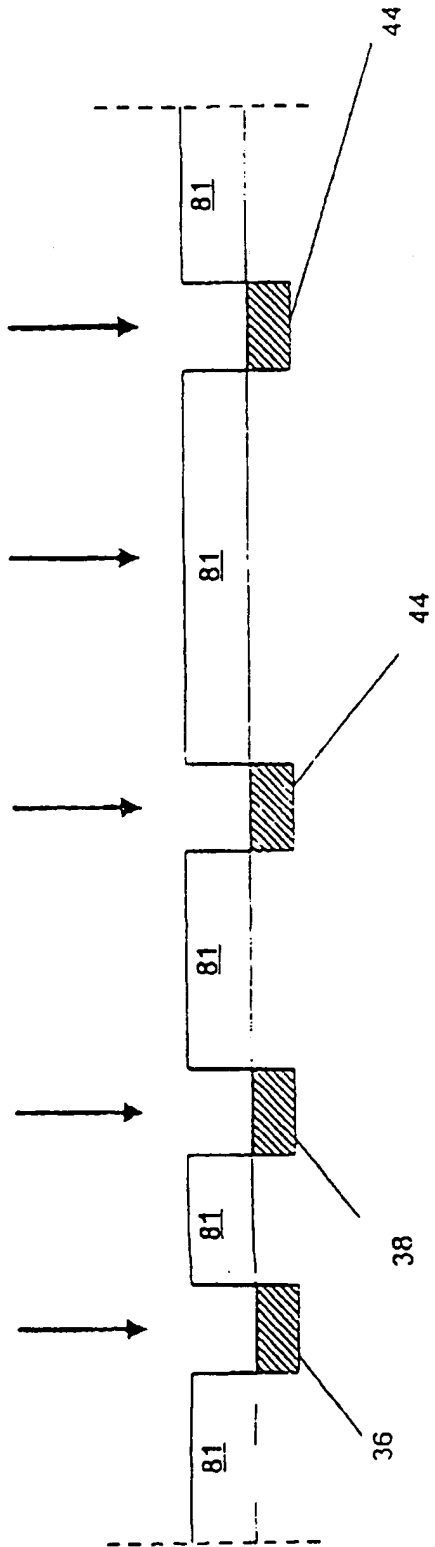


Figure 4

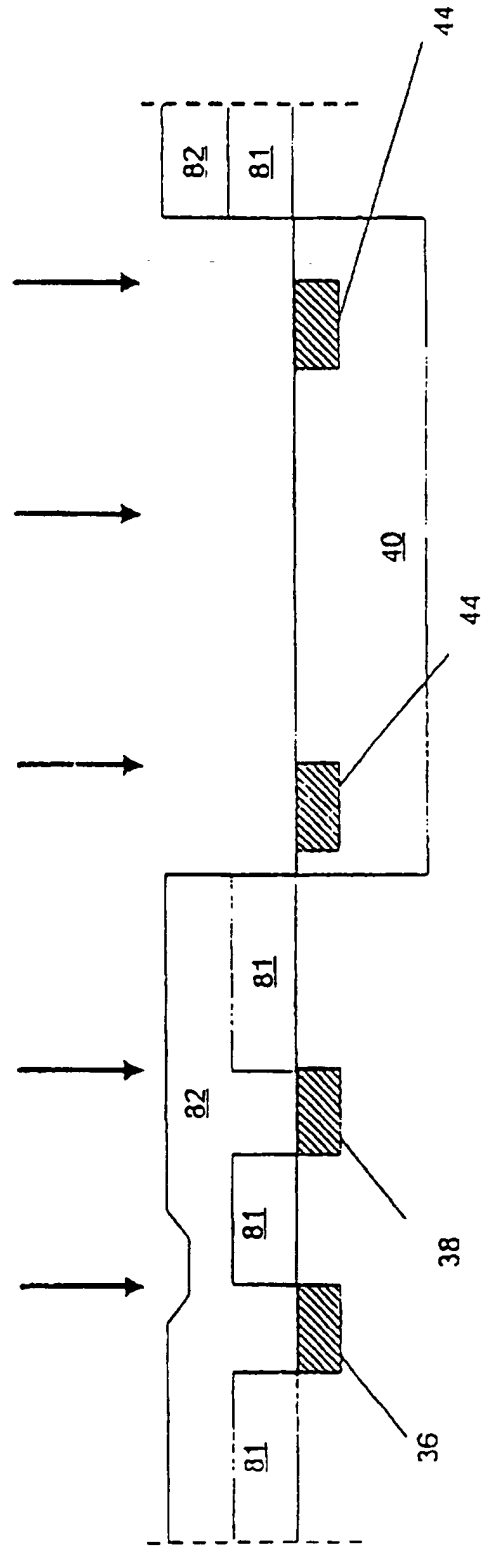


Figure 5

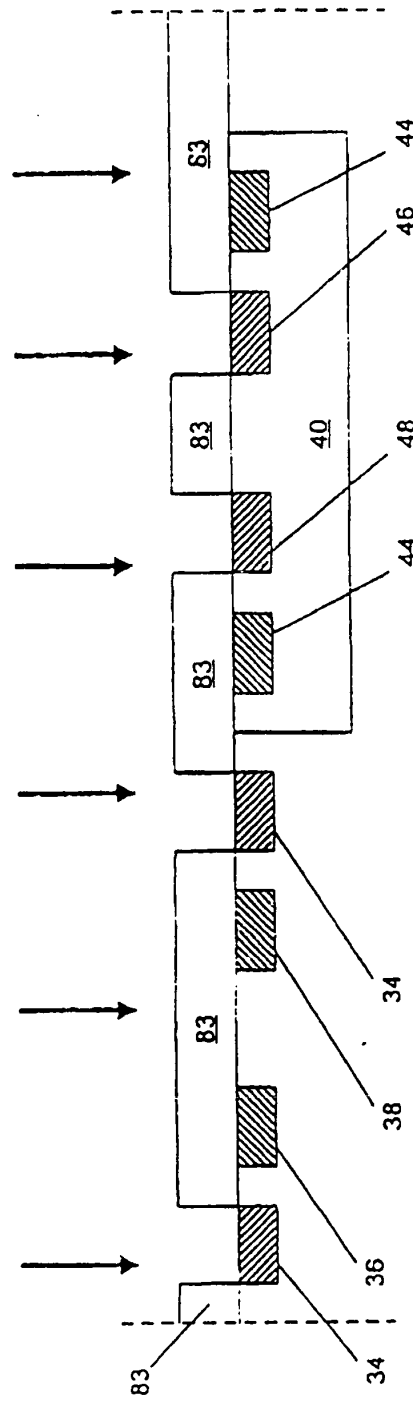


Figure 6

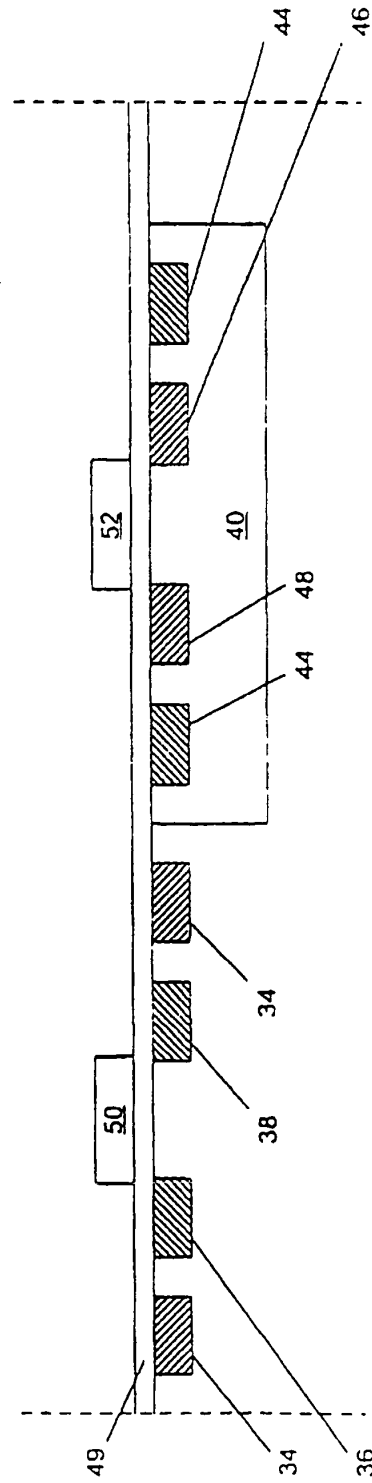


Figure 7

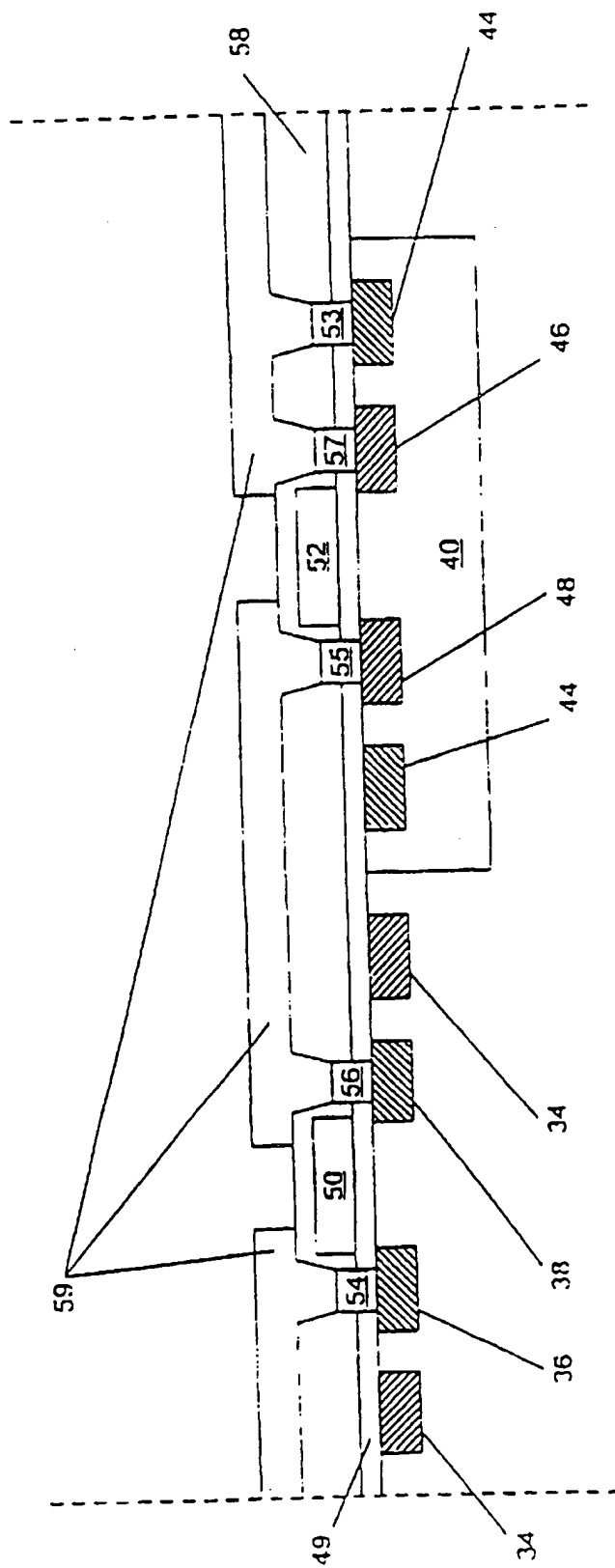


Figure 8

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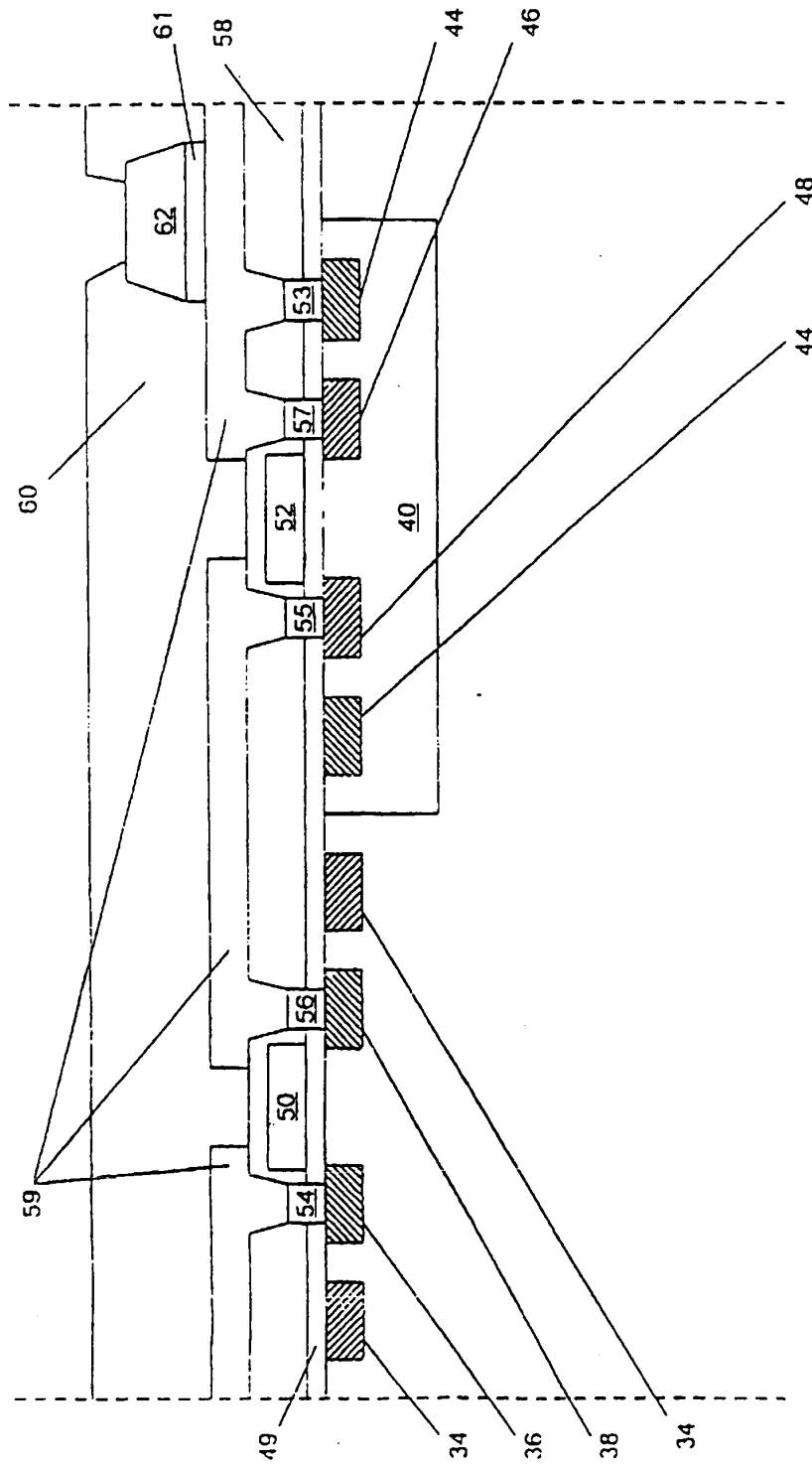
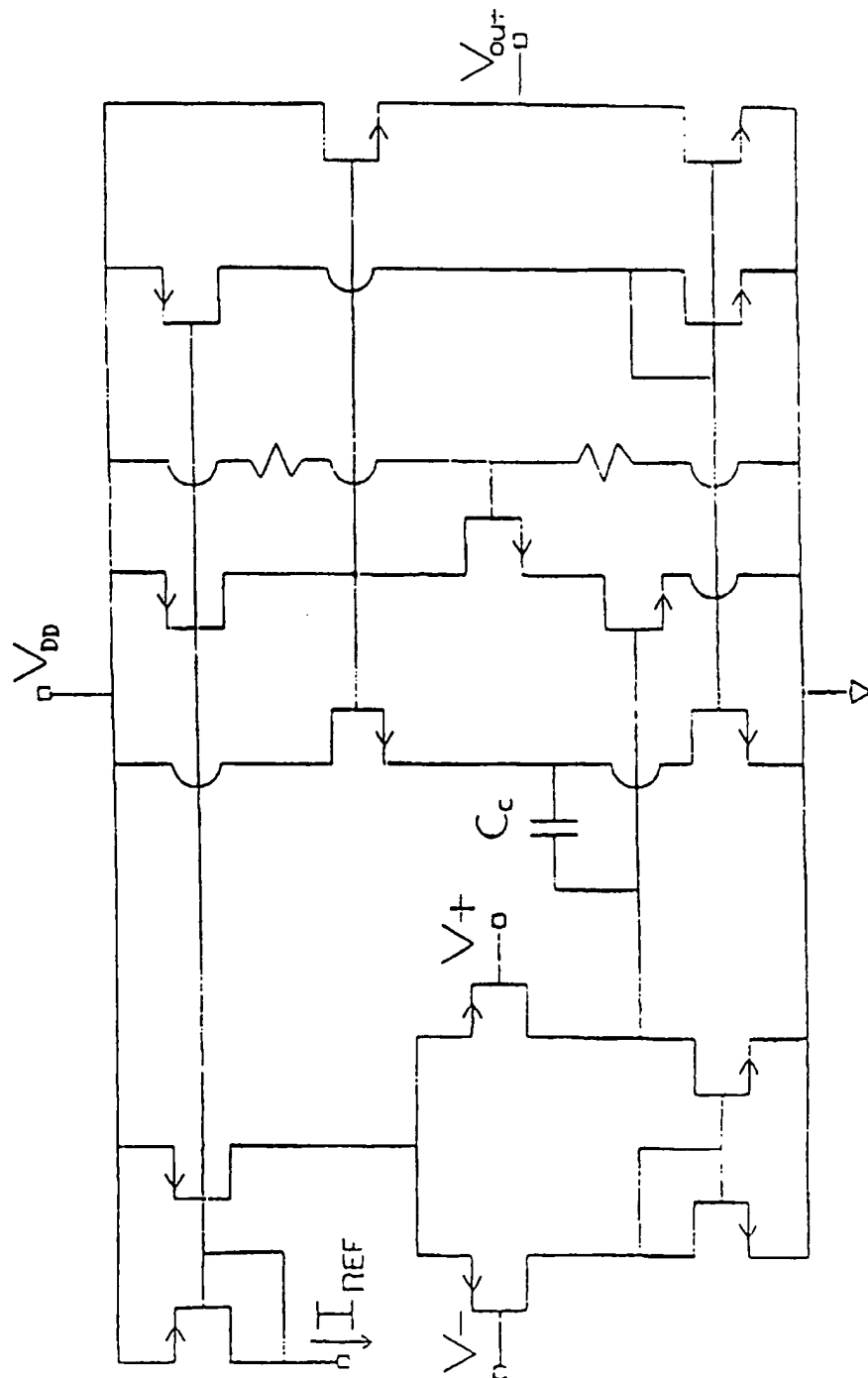


Figure 9

Figure 10





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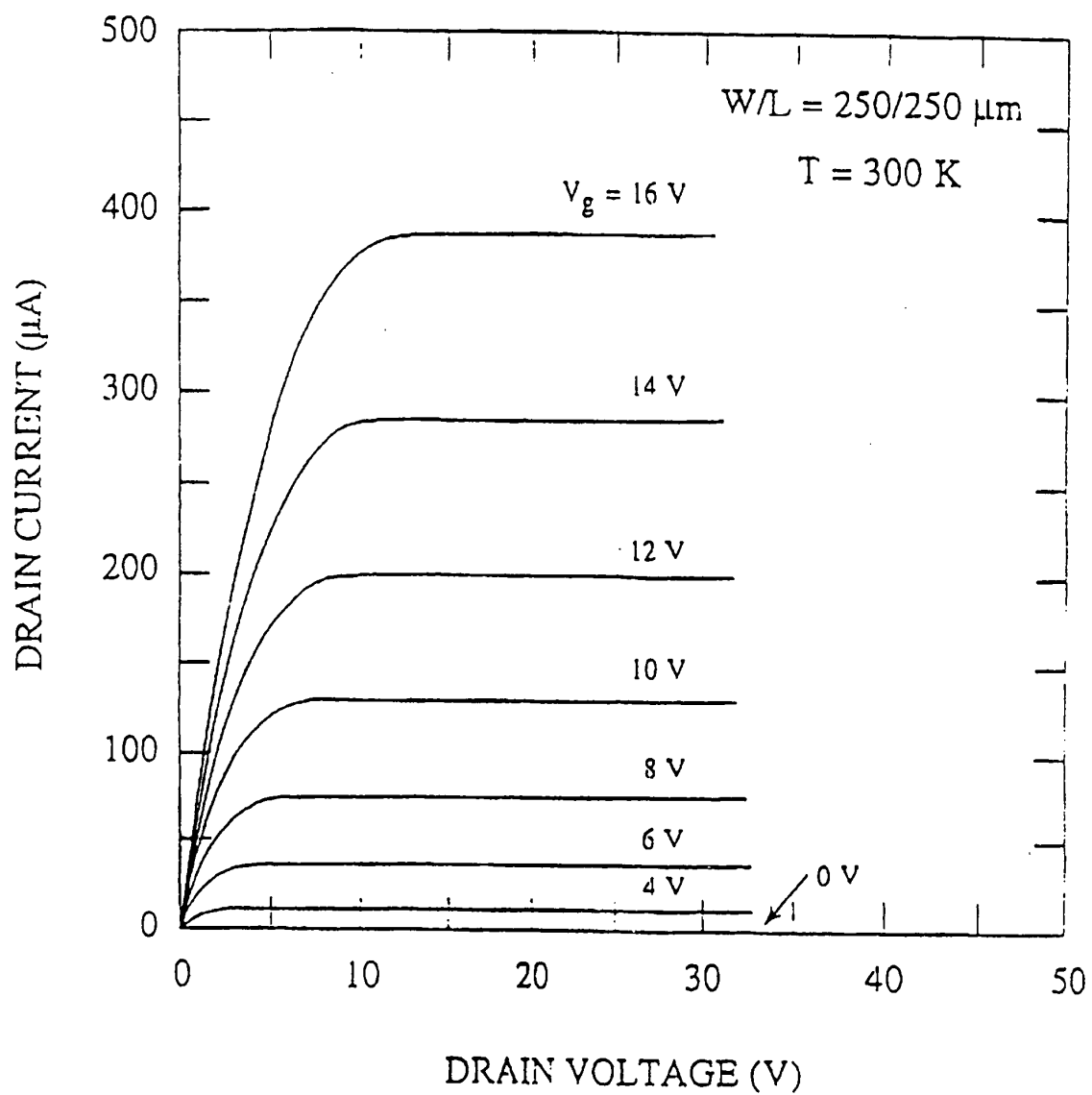


Figure 11A

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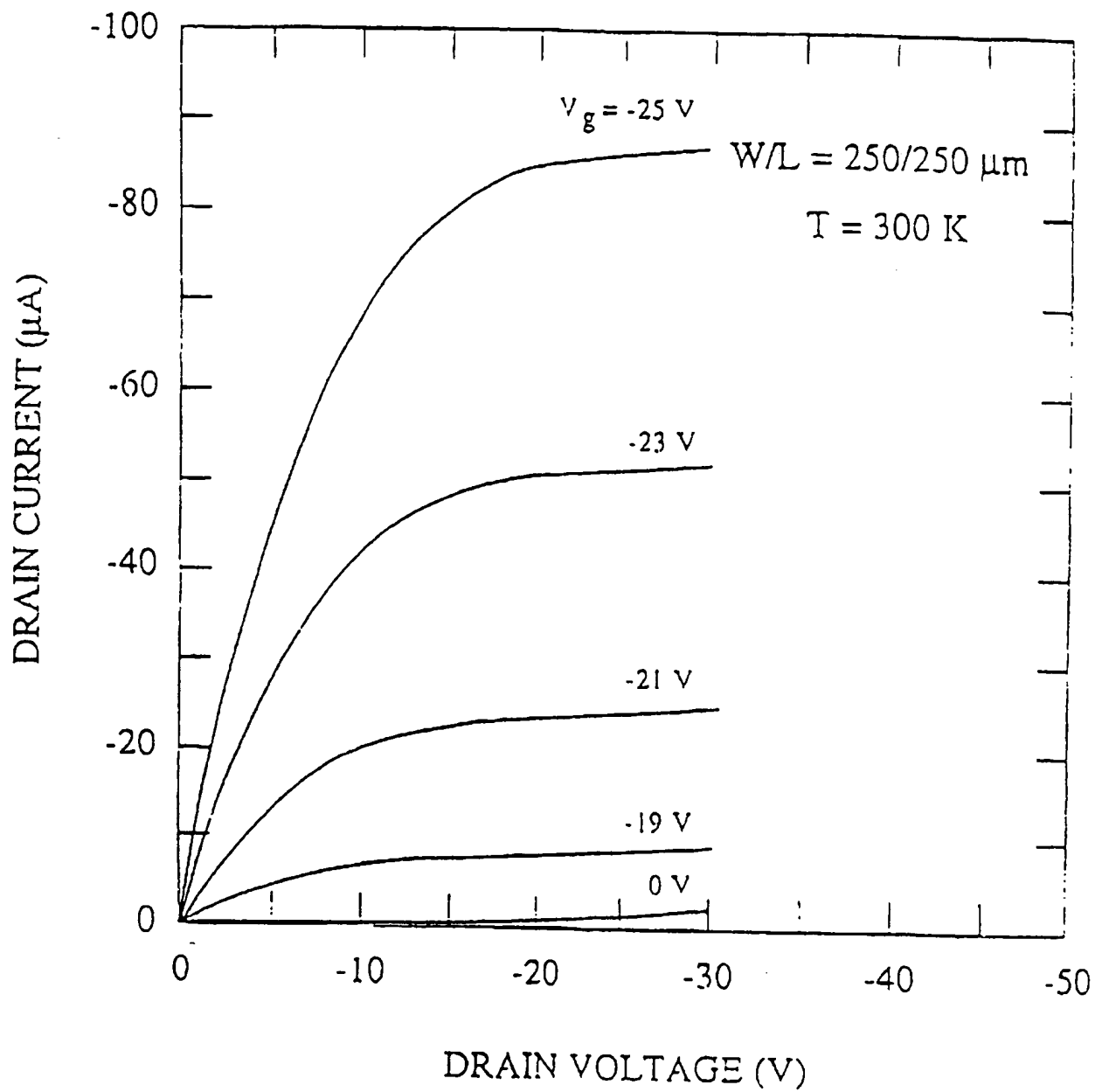


Figure 11B

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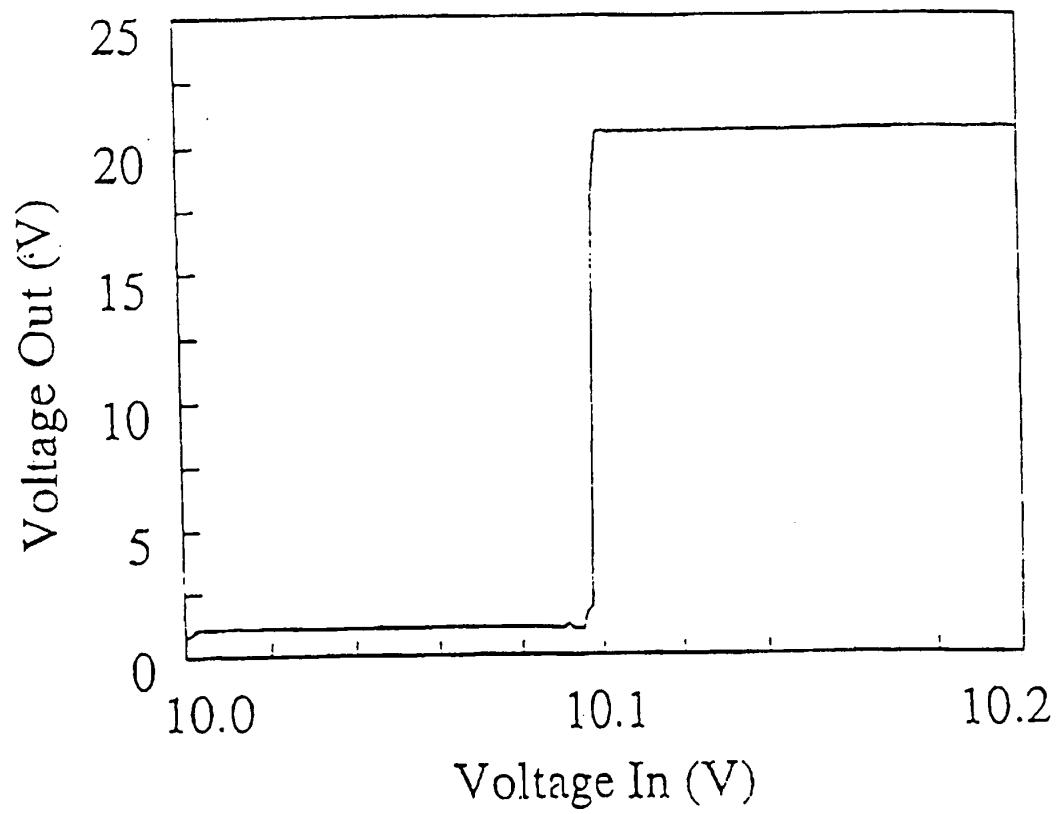


Figure 12

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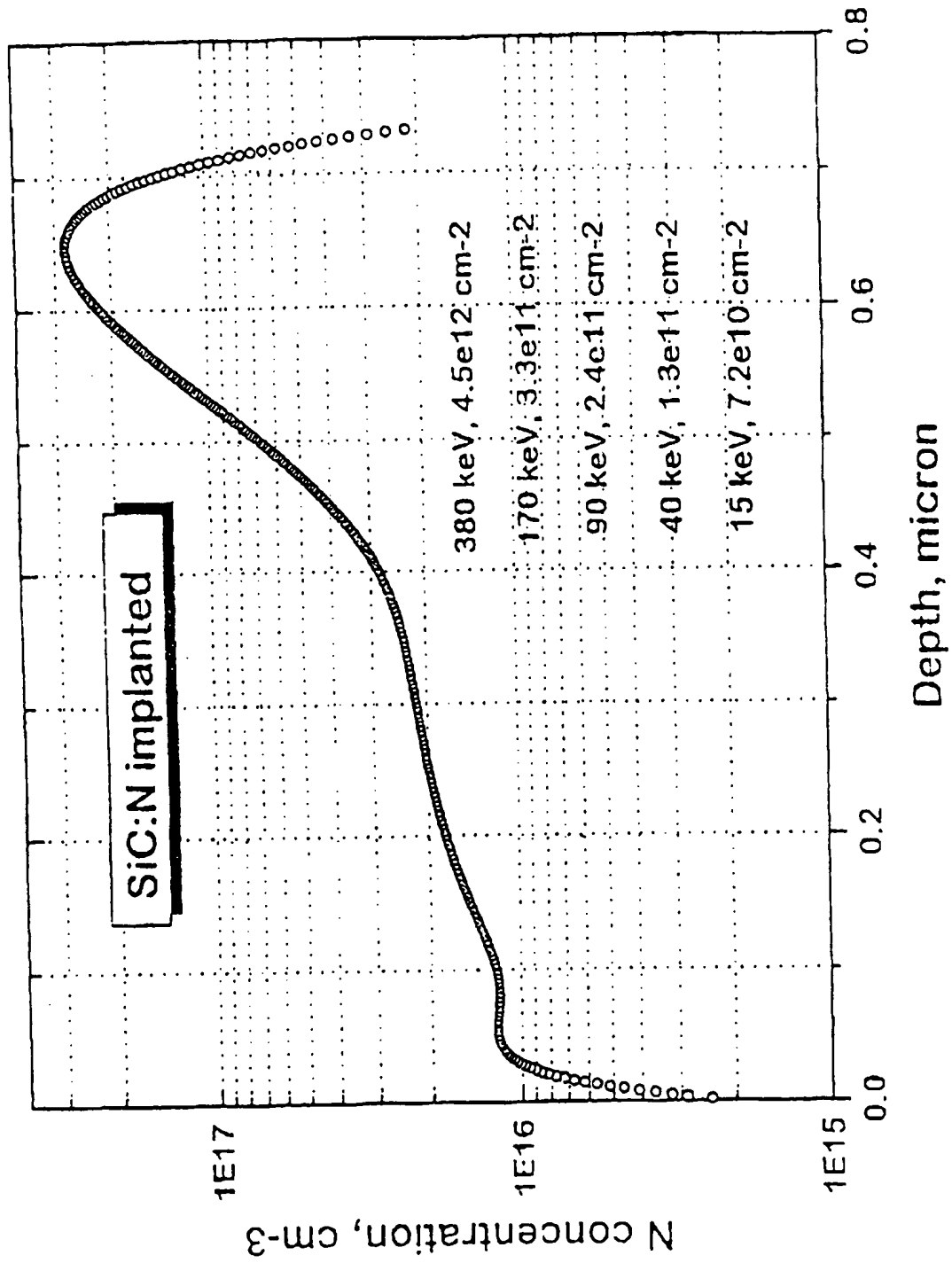


Figure 13

## INTERNATIONAL SEARCH REPORT

In tional Application No

PCT/US 97/06156

A. CLASSIFICATION OF SUBJECT MATTER  
IPC 6 H01L27/06 H01L21/82

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 096, no. 008, 30 August 1996 & JP 08 088283 A (FUJI ELECTRIC CO LTD), 2 April 1996,	1-3,5,6
A	see abstract	14
Y	US 5 385 855 A (BROWN DALE M ET AL) 31 January 1995	1-8, 10-23, 25-33, 35-41
A	see column 2, line 59 - column 6, line 66; figures 1-9	42-45,47
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☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

## \* Special categories of cited documents:

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Date of the actual completion of the international search

11 July 1997

Date of mailing of the international search report

23 -07- 1997

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## INTERNATIONAL SEARCH REPORT

International Application No  
PCT/US 97/06156

## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 342 803 A (SHIMOJI NORIYUKI) 30 August 1994	1-8, 10-23, 25-33, 35-41
A	see column 3, line 36 - column 4, line 29; figures 1A-D see column 6, line 1 - line 60; figures 7A-I	9,24,34, 42-47
A	--- US 5 326 991 A (TAKASU HIDEKI) 5 July 1994  see column 5, line 35 - column 6, line 11; figures 6A-7	1,3,8, 10-12, 16,18,20
A	--- EP 0 372 412 A (FUJITSU LTD) 13 June 1990 see column 8, line 33 - line 51; figure 5E	1
A	--- INST.PHYS. CONF. SER. NO.142: CHAPTER 4; SILICON CARBID AND RELATED MATERIALS 1995, September 1995, KYOTO, JAPAN, pages 805-808, XP002035060 SLATER, D.B. ET AL: "NMOS and PMOS high temperature enhancement mode devices and circuits in 6H-SiC " see abstract	1,7,32
A	--- US 3 849 216 A (SALTERS R) 19 November 1974 see column 9, line 40 - column 10, line 26; figures 14-17 see column 5, line 59 - column 6, line 4; figures 1,2 see column 4, line 11 - line 28 -----	1,2,7, 14,20,42

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information on patent family members

International Application No

PCT/US 97/06156

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